AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph on page 1, lines 5 – 14 with the following amended paragraph.

The present invention is related to U.S. Application Serial No. 10/720,464 (Attorney ~~No. _____~~ ~~(Attorney~~ Docket No. YOR920030358US1) entitled "MULTIPLE VOLTAGE INTEGRATED CIRCUIT AND DESIGN METHOD THEREFOR" to Anthony Correale Jr. et al., U.S. Application Serial No. 10/720,562 (Attorney ~~No. _____~~ ~~(Attorney~~ Docket No. YOR920030359US1) entitled "METHOD AND PROGRAM PRODUCT OF LEVEL CONVERTER OPTIMIZATION" to Anthony Correale Jr. et al., both filed coincident herewith and to U.S. Application Serial No. 10/387,728 (Attorney Docket No. RPS9-2002-0253) entitled "VOLTAGE ISLAND CIRCUIT PLACEMENT" to Anthony Correale Jr., filed March 13, 2003, all assigned to the assignee of the present invention.

Please replace the paragraph on page 9, line 5 – page 10, line 2 with the following amended paragraph.

Figure 4 shows an example of a generic voltage island structure 200 formed using preferred embodiment level converters, wherein different voltages are assigned at both macro and cell levels. Such voltage assignment flexibility affords more freedom in terms of layout style by allowing multiple voltage islands within the same circuit row. Further, such a pattern 200 is achievable with minimum disturbance to an existing placement, i.e., after normal chip design and placement. So, after designing and placing circuits for performance, for example, the design may be modified, selectively replacing higher power (V_{ddh}) circuits (stippled) with lower power (V_{ddl}) circuits (clear) where possible, e.g., as described in U.S. Application Serial No. 10/720,464 (Attorney ~~No. _____~~ ~~(Attorney~~ Docket No. YOR920030358US1) entitled "MULTIPLE VOLTAGE INTEGRATED CIRCUIT AND DESIGN METHOD THEREFOR" to Anthony Correale Jr. et al. (Correale I) and/or U.S. Application Serial No. 10/720,562 (Attorney ~~No.~~

~~(Attorney~~ Docket No. YOR920030359US1) entitled "METHOD AND PROGRAM PRODUCT OF LEVEL CONVERTER OPTIMIZATION" to Anthony Correale Jr. et al. (Correale II), both filed coincident herewith, assigned to the assignee of the present invention and incorporated herein by reference. Since some gap may be needed between adjacent V_{ddl} islands 202 and V_{ddh} islands 204 (depending on the standard cell library), a minimum or maximum allowed cluster size or number of voltage islands may be specified for each circuit row, e.g., 206, based on the particular user or technology specification. See, for example, U.S. Application Serial No. 10/387,728 (Attorney Docket No. RPS9-2002-0253) entitled "VOLTAGE ISLAND CIRCUIT PLACEMENT" to Anthony Correale Jr., filed March 13, 2003, assigned to the assignee of the present invention and incorporated herein by reference. To facilitate power routing, a power grid structure of VDDL 208 and VDDH 210 is co-designed with the voltage island assignment. Preferred embodiment level converters 212 are placed where needed, e.g., in a higher voltage island 204 or with high voltage logic 214.